

A Monolithically Integrated GaN MIS-HEMT DFF Circuit for High Temperature and High Frequency Applications

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Abstract

This paper presents a monolithically integrated D-type flip-flop (DFF) based on GaN MIS-HEMT technology, designed for high-temperature and high-frequency operation. The circuit, employing both depletion- and enhancement-mode MIS-HEMTs, was evaluated up to 200 °C and 500 kHz. Key metrics including propagation delay and signal integrity were characterized. The DFF maintains stable DC margins across 25–200 °C and 1–500 kHz. Rise time increases with frequency from 0.32 μ s at 10 kHz to 0.59 μ s at 200 kHz with little temperature dependence, while fall time show a small variation from 0.13–0.35 μ s. These results demonstrate the feasibility of GaN MIS-HEMT sequential logic under thermal and switching test conditions.

Introduction

Wide-bandgap semiconductor devices, particularly Gallium Nitride (GaN), are becoming increasingly critical in intelligent energy conversion systems due to their low on-state resistance, high breakdown voltage, and excellent high-temperature capability of GaN high-electron-mobility transistors (HEMTs) [1], [2]. Owing to the intrinsic characteristics of the AlGaIn/GaN heterojunction, GaN HEMTs are typically fabricated in depletion mode (D-mode). For fail-safe operation in logic and power systems, enhancement mode (E-mode) devices are required. Various techniques have been developed to achieve E-mode operation, including fluorine ion implantation and recessed gate processing [3], [4]. Recently, metal–insulator–semiconductor (MIS) gate technology has attracted significant interest because it effectively suppresses gate leakage current, improves breakdown voltage, and enhances thermal stability, thereby enabling reliable operation in harsh environments [5], [6].

The D-type flip-flop (DFF) is a fundamental sequential logic element that stores and transfers data synchronously, forming the backbone of registers, counters, and state machines in digital systems. In silicon-based CMOS technology, DFFs are widely deployed in microprocessors and memory architectures due to their mature fabrication process and low static power consumption. However, the operational reliability of silicon-based CMOS circuits degrades significantly at elevated temperatures. Commercial CMOS technologies are typically qualified only within the –40 °C to +125 °C range, beyond which timing instability, increased leakage, and bias temperature instability (BTI) effects become dominant, leading to accelerated performance degradation and potential functional failure [7], [8]. In contrast, monolithically integrated GaN MIS-HEMTs combine wide bandgap, high electron mobility, and reduced parasitic capacitances,

enabling stable sequential logic operation at temperatures beyond 200 °C and in high-frequency regimes [9]. The MIS gate structure further suppresses leakage current and enhances breakdown voltage, making it particularly suited for harsh-environment applications such as aerospace, automotive, and renewable-energy control systems [10].

Zhu et al. [11] reported the monolithic integration of D flip-flop (DFF), using GaN MIS-HEMT technology. Their work experimentally verified correct logical functionality up to 100 kHz with supply voltages of 9 V, highlighting the feasibility of GaN-based MIS-HEMTs for digital integration. Building upon these results, this work investigates, the high-temperature and high-frequency performance of a monolithically integrated GaN MIS-HEMT DFF circuit. Experimental evaluation up to 200 °C and 500 kHz reveals temperature-dependent variations in propagation delay, and signal integrity, providing valuable insight into the timing robustness of GaN-based sequential logic under combined thermal and switching test conditions.

Device Fabrication and Characteristics

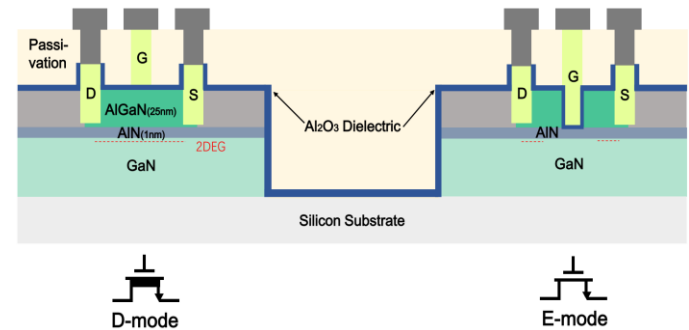


Fig.1 The structure of GaN MISHEMTs.

In the referenced work [12], GaN integrated circuits were fabricated on GaN-on-Si substrates consisting of a 4.2- μ m GaN buffer layer, a 21-nm AlGaIn barrier, and a 1-nm GaN cap. Device isolation was realized through mesa etching, where a 100-nm SiN_x film served as a hard mask during the subsequent recessed-gate formation. A digital etching technique [13] was employed to fully remove the AlGaIn barrier in the recessed regions, thereby achieving enhancement-mode transistors. After the SiN_x mask was stripped using buffered oxide etchant (BOE), Au-free ohmic contacts composed of Ti/Al/Ni/TiN (22.5/90/45/100 nm) were deposited and annealed at 900 °C to form low-resistance source and drain electrodes [14]. A 20-nm Al₂O₃ dielectric layer was then deposited by atomic layer deposition (ALD) for both E- and D-mode devices, followed by Ni/TiN gate

metal evaporation. Finally, a 100-nm SiN_x film was deposited as the intermetal dielectric, and a 200-nm Al layer was patterned to complete the top-level metallization of the GaN IC platform.

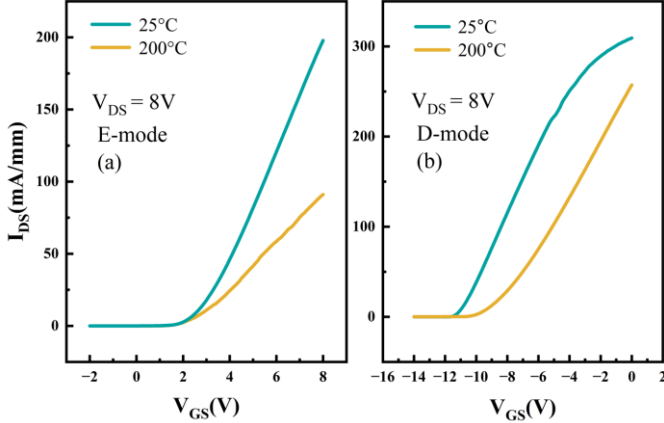


Fig.2 The measured I_{ds} - V_{gs} curves of E-mode (a) and D-mode (b) devices with $V_{ds}=8V$ at various temperatures.

The electrical characteristics of the GaN MISHEMT devices were measured by the Agilent B1500A semiconductor analyzer, and the results are presented in Fig.2. The threshold voltage of the E-mode devices is 1.8 V, while the D-mode device presents a threshold voltage of -13 V. The saturation current of the E-mode device is 197 mA/mm, with D-mode devices at 305 mA/mm at room temperature.

As the temperature rises from room temperature to 200°C, the E-mode devices exhibit a negative drift of approximately 1 V in threshold voltage, while the D-mode devices show a positive drift of about 2 V. Both D-mode and E-mode devices exhibit saturation current decay, with D-mode at 50 mA/mm and E-mode at 100 mA/mm.

For E-mode operation, both the negative threshold voltage shift and the degradation of carrier mobility collectively suppress channel conduction. However, D-mode devices have positive threshold voltage shift. This synergistic effect significantly reduces drain current (I_D) and transconductance (g_m) at fixed gate bias (V_{GS}). The observed trend aligns with the temperature-independent phenomenon also occurs in [12] confirming the critical role of mobility degradation in high-temperature performance.

Threshold-voltage instabilities in GaN MIS-HEMTs are commonly attributed to charge trapping and detrapping at the gate-dielectric/AlGaIn interface and inner-surface defect states, which modulate the effective gate charge and hence shift the threshold voltage. In a simple capacitance picture the change in threshold due to trapped charge Q_{trap} can be expressed as

$$\Delta V_{TH} = -\frac{Q_{trap}}{C_{ox}}$$

where C_{ox} is the gate insulator capacitance per unit area. Experimental and TCAD-assisted studies indicate that E-mode (recessed-gate) devices often exhibit negative V_{TH} shifts linked to gate-injection/detrapping and hole dynamics, whereas D-mode devices show positive shifts caused by electron trapping at Al₂O₃/AlGaIn interface states and stress-induced effects [15, 16].

Circuit structure

As illustrated in Fig.3, a NAND-based D flip-flop (DFF) is implemented using GaN MIS-HEMT technology with a cross-connected SR latch configuration with Direct-Coupled FET Logic (DCFL). The design incorporates eighteen GaN MISHEMT devices, including five D-mode devices (width=25 μ m) and nine E-mode device (width=2000 μ m). The circuit employs five depletion-mode devices (D1–D5) as pull-up/active loads and nine enhancement-mode devices (E1–E9) forming the pull-down network and transmission.

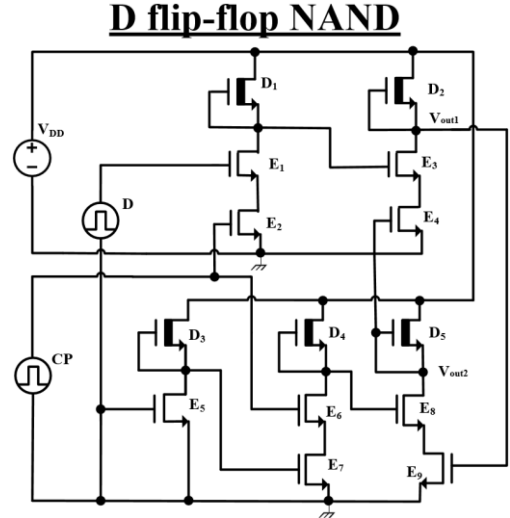


Fig.3 The circuit diagram of the proposed DFF NAND logic gate.

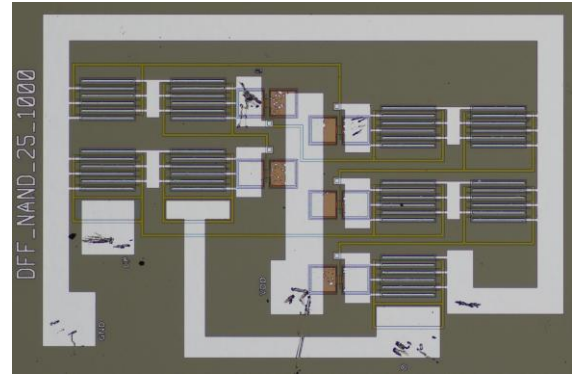


Fig.4 the microphotograph of the proposed GaN DFF circuit.

Operating under a single power supply (V_{DD}), the circuit accepts data input (D) and clock signal (CP), generating complementary outputs (V_{out1}/V_{out2}).

It samples the input D on clock edges and maintains stable latched outputs during respective half-cycles. The use of MIS gate dielectrics suppresses gate leakage currents and enhances static performance, achieving reliable DFF operation with minimal device count and interconnect complexity, suitable for GaN circuit integration.

Experimental Results

The dynamic characteristics were measured by an Oscilloscope. When the supply voltage V_{DD} is at 9V, the measured dynamic waveforms of the NAND-based D flip-flop logic circuit are shown in Fig.5. When the clock pulse signal V_2 is at a logic-low level, V_{out1} retains its previous

state. Once V_2 transitions from logic-low to logic-high, V_{out2} follows the input signal V_1 .

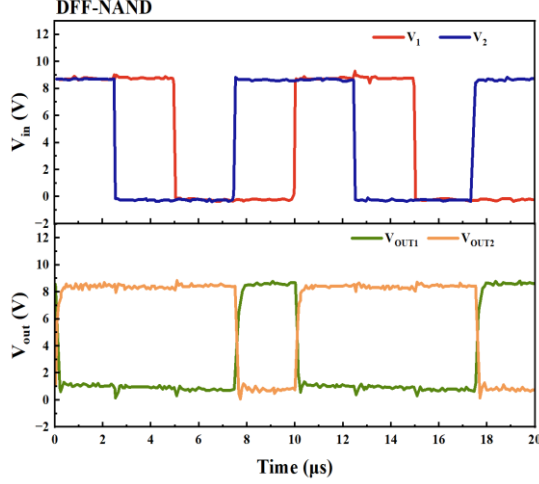


Fig.5 The waveforms of the output voltage of the circuit at room temperature, $f=100$ kHz.

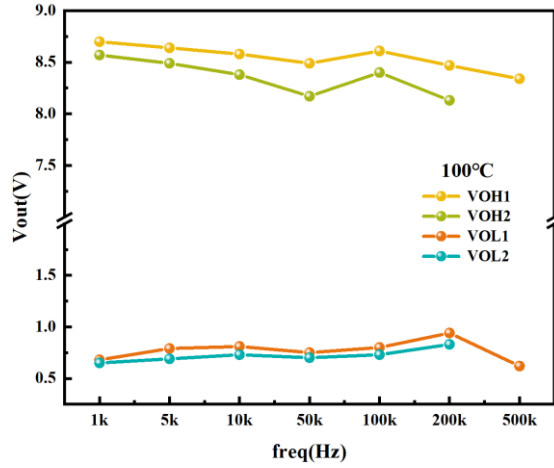


Fig.6 The output voltage at 100°C with various frequencies.

Fig.6 shows the output logic high (V_{OH}) and output logic low (V_{OL}) of the GaN D flip-flop at 100°C . The results indicate that the circuit could maintain its functional operation from 1 kHz to 500 kHz at 100°C . The output logic high voltages slightly decreases with frequency, while the output logic low voltages have no obvious trend.

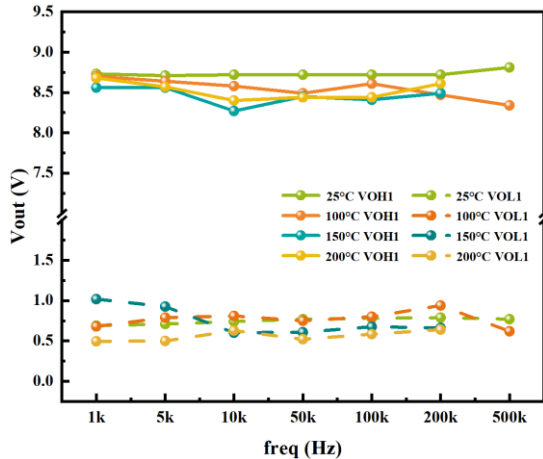


Fig.7 The output voltage at various temperatures and frequencies.

In Fig.7, across 1 k-500 kHz and 25°C - 200°C , V_{OH} remains logic high with small variation, indicating sufficient logic margin. The weak V_{OH} and V_{OL} dispersion with temperature might be caused by the negative shift of the threshold voltage in the D-mode transistor ($\Delta V_{th} < 0$) compensating mobility degradation [10]. The results confirm the high-temperature/high-frequency capability for GaN-based sequential circuits. Hence, this work demonstrates the ability to maintain a relatively stable output under high temperature across various frequencies from 1 kHz to 500 kHz.

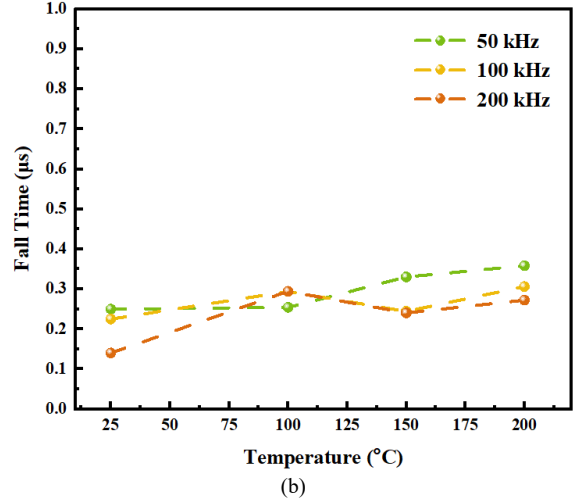
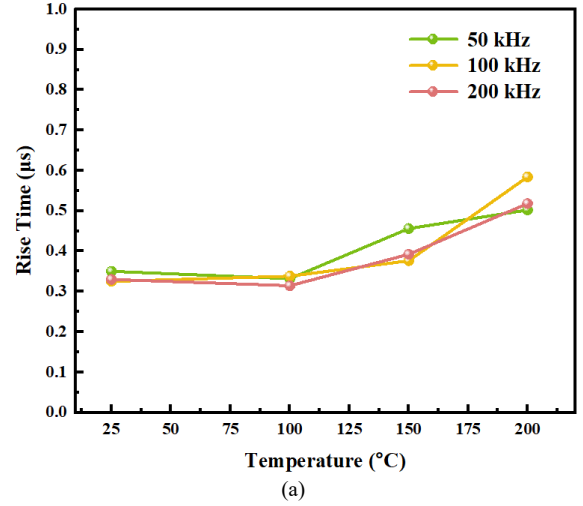


Fig.8 Measured rise time (a) and fall time (b) at 25°C , 100°C , 150°C , 200°C with different frequencies.

In Fig.8, the measured rise time shows an overall increasing trend with temperature, ranging from $0.32\ \mu\text{s}$ at 25°C to $0.59\ \mu\text{s}$ at 200°C at various frequencies. While the fall time shows a variation between $0.13\sim 0.35\ \mu\text{s}$ with no clear trend against temperature or frequency. These results indicate that the DFF output transition is predominantly frequency-sensitive on the rising edge, while the falling edge is largely stable under the tested conditions.

The difference between rise time and fall time might be caused by the variations in threshold voltage shift and mobility degradation between the D-mode device and the E-mode device. The positive shift of threshold voltage in D-mode devices, along with a larger mobility degradation in the

un-recessed channel at elevated temperatures, could cause a more pronounced reduction in charging current, leading to a larger increase in rise time. However, the smaller threshold voltage shift and reduced mobility in the recessed E-mode devices contribute to minimum variation in fall time across different temperatures and frequencies.

Conclusions

A monolithically integrated NAND-based D flip-flop has been experimentally validated from 25 to 200 °C and 1 kHz to 500 kHz. The results indicate that the circuit could maintain large logic margins under various temperatures. Both rise time and fall time exhibit small variation at various temperatures and frequencies. Compared to the rise time increasing from 0.32 μ s to 0.59 μ s as temperature rises, fall time slightly varies between 0.13 μ s and 0.35 μ s, which shows less dependence on temperature and frequency. The results highlight the suitability of GaN MIS-HEMT sequential logic for reliable operation in high-temperature and high-frequency environments.

Acknowledgments

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